



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Heinen
Serial No.: 09/186,973
Filed: 11/05/98
For: **WAFER-SCALE ASSEMBLY OF CHIP-SIZE PACKAGES**

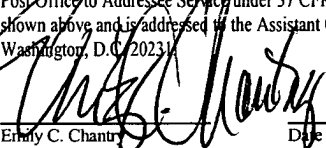
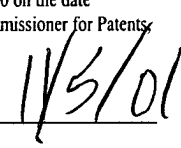
Art Unit: 2823
Examiner: Shukla, R.
Docket: TI-23158

#14/Amend C
Atty
11/1/01
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AMENDMENT 37 CFR 1.115

November 5, 2001

Assistant Commissioner
for Patents
Washington, D.C. 20231

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 Emily C. Chanur	 Date 11/5/01

Sir:

Responsive to the Office Action of July 5, 2001, please amend the application as follows:

In the Claims:

14. (Amended) A method for the fabrication of a semiconductor assembly:

providing a semiconductor wafer [having] comprising a plurality of undivided
integrated circuit[s] chips, each circuit chip having a plurality of metal
contact pads as electrical entry and exit ports;

forming a planar array of solder balls attached to said contact pads of said plurality
of chips on said semiconductor wafer so that each of said contact pads is
contacted by one of said solder balls;

providing an interposer of electrically insulating material having first and second
opposite surfaces and electrically conductive paths from said first [one]
surface to [the opposite] said second surface, forming electrical entry and exit
ports on said insulating interposer;

aligning said interposer with said solder balls so that each port is placed into